IN THE CLAIMS

Applicant submits below a complete listing of the current claims, with any insertions indicated by underlining and any deletions indicated by strikeouts and/or double bracketing.

Listing of the Claims

Please cancel claims 1, 5, 6, and 7 without prejudice or disclaimer.

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Canceled)

2. (Previously Presented) A method of synthesizing a reverse model of a finite state machine, the method comprising:

transforming a transition function of a state machine model of said finite state machine into a constraint on the reverse model, wherein the reverse model is a reverse model of the state machine model; and

applying a parameterization of said constraint to all transitions of the reverse model.

3. (Previously Presented) The method as claimed in claim 2 wherein said finite state machine includes a logic circuits.

4. (Previously Presented) The method as claimed in claim 2 wherein said finite state machine includes a microprocessor.

5. (Canceled)

6. (Canceled)

7. (Canceled)

8. (Currently Amended) A method of calculating a post-image in a finite state machine, the method comprising:

forming a reverse model of said finite state machine, wherein the reverse model is a reverse model of a state machine model of the finite state machine; and

calculating a pre-image in said reverse model, wherein the pre-image in said reverse model is equivalent to the post-image in said finite state machine.

9. (Previously Presented) The method as claimed in claim 8 wherein said finite state machine includes a logic circuits.

10. (Previously Presented) The method as claimed in claim 8 wherein said finite state machine includes a microprocessor.

11. (Previously Presented) The method of claim 8 further comprising identifying from a characterization of a model of said finite state machine, transitions of said finite state machine and reversing said transitions to form potential transitions of a reverse model.

12. (Previously Presented) The method of claim 8 and further comprising extracting from a characterization of a model of said finite state machine, transition functions of said finite state machine.

13. (Currently Amended) A device for synthesizing a reverse model of [[an]] a finite state machine, the device comprising:

a first store storing bits representative of transition functions of a state machine model of said finite state machine;

a second store storing bits representative of an estimate of transition functions of said reverse model; and

a processing system comprising

a logical device for transforming said transition functions of the state machine model of said finite state machine into constraints on said reverse model, wherein the reverse model is a reverse model of the state machine model; and

a parameterization processor for applying a parameterization of said constraints to said estimate of transition functions of said reverse model to form transition functions of said reverse model.

14. (Previously Presented) A device for calculating a post-image in a finite state machine comprising:

a third store storing bits representative of transition functions of a reverse model of said finite state machine;

a fourth store storing bits representative of a set of states of a state machine model of said finite state machine; and

a forming device substituting the state variables of the reverse model by the transition functions of the reverse model to provide a new set of states representing the pre-image of said reverse model, and thus provide the post-image in said finite state machine.

15. (Previously Presented) A device as claimed in claim 14 further comprising a first store storing bits representative of transition functions of said finite state machine;

a second store storing bits representative of an estimate of transition functions of said reverse model;

a logical device for transforming said transition functions of said finite state machine into constraints on said reverse models; and

a parameterization processor for applying a parameterization of said constraints to said estimate of transition functions of the reverse model to form transition functions of said reverse model.

16. (Previously Presented) A device as claimed in claim 13 wherein said estimate of transition functions of said reverse model comprises previous state variables of said finite state machine.

17. (Previously Presented) A device as claimed in claim 15 wherein said estimate of transition functions of said reverse model comprises previous state variables of said finite state machine.

18. (Previously Presented) The device as claimed in claim 13 wherein said finite state machine includes a logic circuits.

19. (Previously Presented) The device as claimed in claim 13 wherein said finite state machine includes a microprocessor.

20. (Previously Presented) The device as claimed in claim 14 wherein said finite state machine includes a logic circuits.

21. (Previously Presented) The device as claimed in claim 14 wherein said finite state machine includes a microprocessor.